

What is claimed is:

1. A video decoding system comprising:

a plurality of transport decoders for receiving compressed
bitstreams of a plurality of channels, parsing and outputting the
5 respective video bitstreams;

a video decoder for receiving the HD-class video bitstreams
of the plurality of channels through the transport decoders, and
decoding a plurality of video frames for a display frame period
in the unit of a picture;

10 an external memory for storing video-decoded frames for a
motion compensation in the video decoder and a dual video
display;

a video display processor (VDP) for reading out the video
frame data of the plurality of channels decoded by the video
15 decoder from the external memory, converting the video frame data
to match a display format, and simultaneously displaying the
video frames of the plurality of channels on a screen of a
display device; and

a memory interface for interfacing the video decoder, the
20 external memory and the VDP so that the video decoder decodes and
displays the plurality of HD-class video frames for the display
frame period.

2. The video decoding system of claim 1, wherein the video decoder comprises:

a video buffer for temporarily storing the video bitstreams of the plurality of channels outputted through the plurality of TS decoders in the unit of a picture, and then outputting the video bitstreams;

a variable-length decoder (VLD) unit for separating the video bitstreams of the plurality of channels outputted through the video buffer into motion vectors, quantization values and DCT coefficients by variable-length-decoding the video bitstreams in the unit of a picture;

a plurality of inverse quantization (IQ) units for inverse-quantizing the DCT coefficients of the respective channels in accordance with the corresponding quantization values;

a plurality of inverse discrete cosine transform (IDCT) units for receiving the DCT coefficients inverse-quantized by the IQ unit, dividing sub-blocks in a macro block including the inverse-quantized DCT coefficients into a plurality of groups, and performing a pipelined IDCT of the groups;

a motion compensation unit for performing a motion compensation of present pixel values in the unit of a picture using the motion vectors outputted from the VLD unit and a previous frame stored in the external memory;

an adder for adding IDCT-transformed values outputted from the respective IDCT units and motion-compensated values outputted from the motion compensation unit; and

5 a picture control unit for controlling the video buffer, the VLD unit, the adder, and the motion compensation unit in the unit of a picture so that other video frames in the display frame period are decoded.

3. The video decoding system of claim 2, wherein the number
10 of the transport decoders, the IQ units or the IDCT units is 2.

4. The video decoding system of claim 3, wherein the memory interface comprises:

15 a down-sampling unit for performing a reduction of an output of the adder in horizontal and vertical directions according to picture and display types, and storing the reduced data in the external memory; and

20 an up-sampling unit for up-sampling data readout from the memory in a horizontal direction during the motion compensation, and outputting the up-sampled data to the motion compensation unit.

5. The video decoding system of claim 4, wherein the down-sampling unit performs a 1/2-reduction of resolution of the

respective pictures in the horizontal direction, or performs a 1/2-reduction of resolution of the respective pictures in the horizontal and vertical directions, respectively, in accordance with the display type of the data outputted from the adder.

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6. The video decoding system of claim 4, wherein the down-sampling unit does not perform a reduction of a DTV main picture, but performs a 1/2-reduction of resolution of a DTV sub-picture in the horizontal and vertical directions if the display type is
10 a PIP type composed of a DTV main display and a DTV sub-display.

7. The video decoding system of claim 4, wherein the down-sampling unit performs a 1/2-reduction of resolution of a DTV main picture and a DTV sub-picture in the horizontal direction
15 only if the display type is a split-screen type composed of a DTV main display and a DTV sub-display.

8. The video decoding system of claim 1, wherein if the input data is encoded to a frame picture and a dual video display
20 is performed, the picture control unit controls so that a period of a decode_sync required for one frame decoding of the video decoder becomes a half period of a disp_field required for one frame display of the VDP, and the plurality of video frames are decoded and displayed for one period of the disp_field.

9. The video decoding system of claim 1, wherein if the input data is encoded to a frame picture and a dual video display is performed, the picture control unit controls so that a period of a decode_sync required for one frame decoding of the video decoder becomes a half period of a disp_field required for one frame display of the VDP, and so that a top field of one channel is decoded for a half period of the decode_sync and a top field of another channel is decoded for the other half period of the decode_sync, while a bottom field of the one channel is decoded for a half period of a next decode_sync and a bottom field of the another channel is decoded for the other half period of the next decode_sync.

10. The video decoding system of claim 1, wherein the external memory comprises a double data rate (DDR) SDRAM having a 64-bit data width of more than 135MHz.